CUSTOMER NO.: 24498
Ser. No. 10/581,873
Final Office Action dated: 08/13/09
Response dated: 11/13/09

Remarks/Arguments

In the Final Office Action dated August 13, 2009, it is noted that claims 1-14 are pending and that claims 1 and 3-14 are rejected. Claims 1 and 13 are independent. Claim 2 is considered to be allowable subject matter.

On page 9 of the Office Action, the Examiner alleges that the "at least two memory bank commands" described in the preamble of claim 1 are not specifically referred to in the body of the claims, and as such, the commands in the preamble and the commands in the body of the claim may be interpreted as different commands.

Claims 1-5 and 13 have been amended to recite in the body "the at least two memory bank commands...". This amendment clarifies that the commands transmitted via multiple channels are the commands needed for data exchange between the IC and the RAM. Therefore, the commands in the preamble and the commands in the body may not be interpreted as different commands. No new matter has been added to the specification or claims.

35 USC §103(a)

Claims 1, 3, 4, 6, 7, 10, 13 and 14 stand rejected under 35 USC §103(a) as unpatentable over Mes (US 7,028,142) in view of Zeravleff (US 5,630,096). The Applicants respectfully traverse these rejections.

In re Wada and Murphy, Appeal 2007-3733, the BPAI stated that:

> When determining whether a claim is obvious, an examiner must make "a searching comparison of the claimed invention – *including all its limitations* – with the teaching of the prior art." *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis added). Thus, "obviousness requires a suggestion of all limitations in a claim." *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (*citing In re Royka*, 490 F.2d 981, 985 (CCPA 1974)). Moreover, as the Supreme Court recently stated, "*there must be some articulated reasoning* with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (quoting In re Kahn, 441 F.3d 977, 988 (Fed. Cir. 2006) (emphasis added)).

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In the Final Office Action, page 9, the Office responds to applicants' prior arguments. The Office argues that the claims do not draw a distinction between an "instruction" and a "command" and also argues that the "at least two memory bank commands," described in the preamble of claim 1, are not specifically referred to in the body of the claims.

As amended, claim 1 now recites: "transmitting the at least two memory bank commands via multiple channels", and each additional feature in claim 1 provides antecedence to the prior commands. Thus, the "at least two memory bank commands" is specifically referred to in the body of the claims.

Furthermore, applicants contend that with this additional clarification the distinction between and "instruction" as described by Mes and applicants' claimed "commands" is clear because claim 1 recites: "where data exchange between the IC and the external RAM necessitates at least two memory bank commands" (the at least two memory bank commands being referred to in the body of the claim as pointed out above).

As previously discussed by applicants, Mes describes instructions because Mes is directed to a shared program memory 102, which is shared by more than one processor 104. A round robin algorithm is applied. A fetch buffer 152 and a prefetch buffer 154 for storing a plurality of instructions being used by the associated processors 104 are disclosed. Arbitrators 108, 202, 204, 206, 208 for arbitrating between a plurality of instructions are disclosed.

Examples of an "instruction" are given in the specification as "branch" or "jump" (column 1, lines 38-39). It can be seen that an instruction is a logical action of memory access. Instructions needs several steps to be performed. Each step is initiated by a command.

Mes does not disclose or suggest anything with regard to arbitrating commands needed to be sent for specific instructions.

One ordinarily skilled in the art would understand based on common knowledge of the ordinarily skilled person and from Mes that, for example, a write instruction needs several steps. One step is to activate the corresponding row in the memory, which is

done by an Activate command. The next step is to initiate the data transfer by transmitting the write command together with the column address in the memory. This is done by a Write command. Afterwards, a precharge command has to be sent to deactivate the open row and reset the memory (page 2, line 25 to page 3, line 2). Therefore, claim 1 does distinguish the "instruction" from a "command" since claim 1 recites: "data exchange between the IC and the external RAM necessitates at least two memory bank commands."

Because Mes fails to teach or suggests "commands" as recited in claim 1, it follows that Mes likewise does not teach or suggest the prioritizing the transmitted commands on the basis or static priority allocation, and further prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels.

As pointed out in the Office Action page 3, Mes discusses using a round-robin fetch arbiter for the instructions from the different processors. There is no discussion of prioritizing commands as in claim 1.

In addition the Office Action on page 3 concedes that Mes fails to teach the feature of the data exchange between the IC and the external RAM necessitates at least two memory bank commands, and alleges that Zuravleff at column 5 lines 2-5 provides this teaching. The Applicants have considered Zuravleff in its entirety and respectfully disagree with this allegation.

Zuravleff at column 5 lines 2-5 discloses that memory requests are resolved into their required sequences of precharge/bank activate/read-write sequences and placed in a queue. However, there is no suggestion in Zuravleff that the commands are prioritized on a static basis and further that a dynamic prioritizing scheme is used for the channels, which transmit the commands. In addition, Zuravleff does not close the gap between Mes and the present claim 1, because Zuravleff only discloses that multiple commands are needed for accessing a RAM memory.

Claim 1 recites that at least two memory bank commands for data exchange between the IC and the external RAM, transmitting the commands via multiple channels, prioritizing the commands on the basis of a static priority allocation, and further prioritizing the commands having the same static priority on the basis of a

dynamic priority allocation for the channels, while in contrast, Zuravleff merely discloses the commands needed for a memory access instruction, whereby the commands may be issued out of order. Nowhere does Zuravleff disclose or even suggest a method for communication between an IC and an external RAM whereby the commands for accessing the memory can be prioritized according to the Applicants' prioritization scheme to sort the pending commands according to their ability to start a new burst in such a way that optimum use of the DRAM data bus is achieved.

As such, a person with ordinary skill in the art would realize that the combination of Mes and Zuravleff's computer executable commands are different from the Applicants' claim 1 and are not applicable to the Applicants' claimed invention.

Additionally, the Office action on page 4 simply puts forth a conclusory statement with regard to it being obvious to have implemented Zuravleff's two commands for memory access instruction for use in the data exchange between the IC and the external RAM. As pointed out above, Zuravleff is different from the Applicants' claimed invention because Zuravleff does not suggest a method for communication between an IC and an external RAM whereby the commands for accessing the memory can be prioritized according to the Applicants' prioritization scheme.

According to the Examination Guidelines for determining Obviousness under 35 U.S.C. 103 in view of the Supreme Court Decision in *KSR international co. V. Teleflex Inc.* ("Guidelines" effective October 10, 2007), the proper analysis of determining obviousness is whether the claimed invention would have been obvious to one of ordinary skill in the art after consideration of all the facts. KSR requires that an Examiner provide "some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness." (KSR Opinion at p. 14). An Examiner must "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does," (KSR Opinion at p. 15). And, the Examiner must make "explicit" this rationale of "the apparent reason to combine the known elements in the fashion claimed," including a detailed explanation of "the effects of demands known to the design community or present in the marketplace" and "the background knowledge possessed by a person

having ordinary skill in the art." (KSR Opinion at p. 14). Anything less than such an explicit analysis may not be sufficient to support a prima facie case of obviousness.

The Office Action fails to provide any of the reasoning required by the MPEP or case law. Nor is there any suggestion making such a combination. Accordingly, the claimed invention has the advantage of using priority allocation scheme to optimize the use of the DRAM data bus. As such, after consideration of all the facts, it would not have been obvious to a person with ordinary skill in the art to combine Mes and Zuravleff as a basis for the rejection under 35 USC 103(a).

Claim 1 patentably distinguishes over Mes and Zuravleff, separately or in combination. As such, the Applicants respectfully maintains that the rejection of claim 1 under 35 U.S.C. 103(a) over Mes and Zuravleff is unfounded and should be withdrawn.

Independent claim 13 is different from claim 1 and must be interpreted differently; however, claim 13 includes apparatus features substantially similar to those found in claim 1. Thus, it is also submitted that the combination of Mes and Zuravleff does not teach, show, or suggest all the elements of Applicants' claim 13, as such, claims 1 and 13 full satisfy the requirements of 35 U.S.C. § 103 and are patentable there under.

Claim 5 stands rejected under 35 USC §103(a) as unpatentable over Mes and Zeravleff in view of Kuddes (US 5,418,920). Claim 8 by Mes and Zeravleff in view of Chen (US 2003/0051108). Claim 9 by Mes and Zeravleff in view of Wheeler (US 6,983,350).

Claim 11 by Mes and Zeravleff in view of LaBerge (US 2001/0044885). Claim 12 by Mes and Zeravleff in view of the power point entitled "Random Access Memory."

Claims 3, 4, 6, 7, 10 depend from claim 1 and include all the features discussed above with respect to claim 1. Claim 14 depends from claim 13 and includes all the features discussed above with respect to claim 13 (claim 1). Thus, it is respectfully submitted that these dependent claims are likewise allowable for the above reasons and because they each include additional features.

With regard to the remaining dependent claims it is respectfully submitted that none of the further references teach the features lacking in the combination of Mes and Zuravleff as discussed above. Thus, the Applicants essentially repeat the above arguments for each dependent claim and respectfully request each rejection be withdrawn.

Conclusion

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the Applicants' attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against Deposit Account No. 07-0832.

Respectfully submitted,

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November 13, 2009